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TITLE: A DEMODULATION APPARATUS OF A BASE STATION IN A CDMA MOBILE COMMUNICATION SYSTEM

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A DEMODULATION APPARATUS OF A BASE STATION IN A CDMA MOBILE COMMUNICATION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a base station in a Code Division Multiple Access (CDMA) mobile communication system, and more particularly, to a demodulation apparatus of a base station in CDMA mobile communication system.

2. Background of the Related Art

Quadrature Phase Shift Keying (QPSK) demodulation in a mobile communication system may be accomplished by converting a high frequency signal received via an antenna into an intermediate frequency signal by using a mixer, and dividing the intermediate signal into an In-Phase channel (I channel) and a Quadra-Phase channel (Q channel) before demodulating to a base-band frequency signal with a demodulator. The analog base-band frequency signal thus demodulated into I and Q channels using the QPSK demodulation is then adjusted to a specific amplitude using a Low-Pass filter and an amplifier. Next, the signal is converted into a base-band digital signal, which is a CDMA signal, using an analog-to-digital converter. Finally, the CDMA signal is transferred to a CDMA modem for demodulation.

separate into I + Q signals

Figure 1 shows a block diagram illustrating a related art base station receiver of a mobile communication system. Referring to Figure 1, a signal transmitted from a mobile station is received through the base station antenna and relayed to a low noise amplifier 103 via the channel-pass filter 102. The low noise amplifier 103 then amplifies and outputs the signal, and passes it through the band-pass filter 104 and the high frequency amplifier 105. Next, the signal is converted into an intermediate frequency CDMA signal in the high frequency mixer 106.

The intermediate frequency CDMA signal then passes through a Surface Acoustic Wave (SAW) filter 107 and the intermediate frequency amplifier 108 to remove unnecessary signal components. The resulting signal is transmitted to the QPSK demodulator 109 where it is demodulated. The QPSK demodulator 109 outputs an I channel signal and a Q channel signal.

The high frequencies of the analog I channel and Q channel signals as demodulated by the QPSK demodulator 109 are removed by the low-pass filter 110. The filtered signals are then amplified by the base-band amplifier 111 to a specific amplitude compatible with the analog-to-digital conversion, and subsequently transferred to the Analog-to-Digital converter 112.

The Analog-to-Digital converter 112 converts the transmitted signal into a base-band digital signal. The base-band CDMA signal (i.e., the I channel and the Q channel converted to digital signals) is relayed to a CDMA modem 113 for demodulation.

Thereafter, the demodulated CDMA signal is transferred to the central office 114, for example a switching station, as a Pulse Code Modulation (PCM) signal.

The QPSK demodulation method of the related art system, however, has various problems. For example, the signal is divided into the analog base-band frequency signal with an I channel and a Q channel by the QPSK demodulator 109, and the divided signal is converted to the digital signal using the Analog-to-Digital converter 112. As a result, numerous circuit devices are needed, making the circuit diagram is more complex, more expensive, and less efficient.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a demodulation system that substantially obviates one or more of the problems caused by the disadvantages of the related art.

Another object of the present invention is to provide a demodulator that can perform Quadrature Phase Shift Keying (QPSK) modulation and Analog-to-Digital Conversion using only a Analog-to-Digital Converter.

Another object of the present invention is to provide an apparatus for base station demodulation of a CDMA mobile communication system that can directly perform the QPSK demodulation and Analog-to-Digital Conversion using only an Analog-to-Digital Converter of a QPSK receiver compatible with the mobile communication system.

Another object of the present invention is to provide a demodulation system for a base station in a mobile communication system which is power efficient and cost effective.

To achieve at least the above objects in whole or in part, there is provided an apparatus for the base station demodulation in a CDMA mobile communication system having an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provide a quadrature component and an in-phase component of the digital signal, a plurality of filters to filter the components of the digital signal in the low pass band respectively, and a CDMA modem to demodulate the outputs of the plurality of filters.

To achieve the above objects in whole or in part, there is further provided a signal processing device having a digital sampling device to sample the transferred intermediate frequency signal, a signal arbiter to distinguish the amplitude of the intermediate frequency signal passed through the digital sampling device, and a quantization device to convert the distinguished intermediate frequency signal to a digital signal, a latch device to hold the converted digital signal for a specific period of time before transferring to a plurality of channels, and an output device to transfer the digital signal to each channel of a plurality of channels to a plurality of filters at the specific transfer periods.

To further achieve the above-described objects of the present invention in a whole or in parts, there is provided a signal processor that includes a digitizer, which receives

and analog signal and generates a digital signal, a channel separator, which receives the digital signal from the digitizer and separates the digital signal into at least 2 channels, each channel having a different phase, and a phase shift controller, which receives a clock signal and controls the phase shifting of the channel separator.

To further achieve the above-described objects of the present invention in a whole or in parts, there is provided a demodulator for a CDMA receiver that includes an input circuit to amplify a filtered CDMA formatted input signal, a first signal processor to generate an intermediate frequency CDMA signal based on the amplified input signal, a second signal processor to output first and second digital signals on first and second channels, respectively, based on the intermediated frequency CDMA signal, the second signal processor having an analog-to-digital converter to convert the intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate the first and second digital signals based on the intermediate digital signal, and an output circuit to output a demodulated output signal based on the first and second digital signals, the output circuit having first and second Finite Impulse Response (FIR) filters to receive and filter the first and second digital signals, respectively, wherein the first and second digital signals have different phases.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having

ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention my be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

Figure 1 is a block diagram of a related art mobile communication system.

Figure 2 is a block diagram showing a CDMA mobile communication system with a base station demodulation apparatus in accordance with a preferred embodiment of the present invention.

Figure 3 is a block diagram showing the Analog-to-Digital converter of Figure 2.

Figure 4 is a block diagram showing the internal circuit of the output formatter of Figure 3.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 2 illustrates the base station demodulation apparatus for a CDMA mobile communication system according to a preferred embodiment of the present invention. Elements 201 through 208 are similar to the related art base station receiver of the mobile communication system of Figure 1. The system as shown in Figure 2, however, uses an

Analog-to-Digital converter 209 as a signal processing device to perform both QPSK demodulation and Analog-to-Digital conversion.

As illustrated in Figure 3, the Analog-to-Digital converter 209 of the signal-processing device preferably includes a digital sampler 301 to sample the intermediate frequency signal received from the intermediate frequency amplifier 208, and a zero-order holder 302, which serves as a signal arbiter for distinguishing the amplitude of the intermediate frequency signal sampled by the digital sampler 301. A quantizer 303 then converts the distinguished intermediate frequency signal to a digital signal.

First, second, and third latch devices 304, 305 and 306 delay the converted digital signal for a prescribed time period before transferring it to a plurality of channels, for example, an I channel and Q channel, by way of first and second formatters 307 and 308. The first and second formatters 307 and 308 in turn periodically transmit the channel divided digital signals to a corresponding plurality of filters 210. The filters are preferably low pass filters, for example, a Finite Impulse Response (FIR) low pass filter. The system further includes a plurality of buffers 310 for buffering the transferred signal, and a D flip-flop 311.

Referring to Figure 4, the first and second formatters 307 and 308 are preferably provided with a plurality of negators 401 for negating the transferred signal and outputting the signal, and a plurality of selectors 402 of selecting one of the output signals of the negator 401 and the signal that has not passed through the negator 401.

The demodulation process of the base station signal will now be described. Referring to Figures 2 and 3, the CDMA analog signal transferred to the Analog-to-Digital converter 209 from the intermediate frequency amplifier 208 is sampled by the digital sampler 301. At this time, the prescribed sampling frequency is preferably twice the frequency of the sampling clock of the desired base-band frequency subtracted from the transferred intermediate frequency. The selected clock frequency, however, is established so as to avoid Aliasing and the clock selected for the bandwidth of the base-band signal should be over the Nyquist rate.

"Aliasing" must be considered when the sampling signal is recovered. Aliasing occurs when the original signal cannot be distinguished or properly reconstructed due to an overlap of the recovered signal. When aliasing occurs, the original signal takes on the identity of a lower frequency, and information can be lost. That is, when the sampling frequency is lower than twice the signal bandwidth of the signal that is being repeatedly generated at the sampling period rate in a Fourier domain, the original signal begins to overlap itself. The original signal thus cannot be reconstructed even if a filter is used. Therefore, after the analog signal is converted to the digital signal, the digital signal can only be transformed back to the original signal using a sampling frequency over the Nyquist rate.

In order to convert the continuous analog input signal that has been passed through the above-described sampling process into the digital signal, a zero-order-hold circuit 302

is used, which distinguishes the amplitude of the signal, preferably at discrete time points. The sampling signal, which is preferably in the form of a discrete time signal, is a continuous signal component repeatedly inputted at a prescribed frequency, generates the digital signal of the proper value according to the amplitude of the input signal.

At the same time, the under-sampling process occurs as the transferred clock frequency is inputted to the buffer 310. The under-sampling process is a process which applies the analog demodulation process to the digital demodulation process and intentionally aliases the signal. Generally, when the signal demodulated with the high frequency is converted by Analog-to-Digital conversion, it is sampled with the clock having a frequency of more than twice the corresponding frequency (the Nyquist Rate) to generate the digital signal. However, in the case of the under-sampling process, demodulation of the under frequency is accomplished at the same time as the Analog-to-Digital conversion takes place by using the Analog-to-Digital clock (which has a frequency of more than twice the bandwidth of the demodulated signal) with the frequency lower than that of the modulated signal.

The under-sampling process occurs when the analog demodulation process is applied to the digital demodulation process. In general, when the signal modulated to the high frequency is converted from analog to digital, the clock having more than twice the subject frequency is used for the sampling to digitize the signal. In the case of the under-sampling, the clock with more than twice the frequency of the bandwidth of the signal

demodulated to the lower frequency than the modulated signal is used as the analog-to-digital clock, and the under demodulation of the frequency is performed at the same time as the analog-to-digital conversion takes place. The output frequency of the quantizer 303 is repeatedly performed throughout all band areas in the sampling frequency periods during the sampling process. Therefore, among the output frequency of the quantizer 303, only the output frequency of the base-band quantizer is allowed to pass through the low-pass filter 210 to perform the demodulation process.

The clock inputted to the buffer 310 is supplied to the first and second output formatters 307 and 308 after the D flip-flop 311 performs a binary counting procedure. The output of the latch B 306, which is shifted one clock period from the output of latch A 305, is latched again to 0.5 times the frequency of the quantization output frequency. As a result, a QPSK demodulation signal shifted 90° out of phase with twice the periodic occurrences of the transmitted clock can be obtained.

The CDMA digital signal converted by the analog-to-digital converter is latched by the latch 304 at more than twice the sampling periods transferred to the I channel and Q channel, before being transmitted to the latch A 305. The latch A 305 then transfers the I channel signal of the transferred base-band digital CDMA signal to a Finite Impulse Response (FIR) low-pass filter 210 at the desired base-band transferred periods via the first output formatter 307.

The Q channel is inputted to the latch B 306, and as the same latched signal having a delay of one sample period with a phase difference of 90° to the I channel having twice the sampling period is transferred to the second output formatter 307, the same function as the analog QPSK is accomplished.

That is, in the low-pass FIR filter 210, the unnecessarily repeated signal components generated during the "under-sampling process" and "Analog-to-Digital Conversion process" are removed before the base-band digital CDMA signal is transmitted to the switching station 212 through the PCM signal via the CDMA modem 211.

As described above, the base station demodulation apparatus of a CDMA mobile communication system in accordance with a preferred embodiment of the present invention has several advantages. For example, the digital signal of I channel and Q channel of the base-band can be directly demodulated in the intermediate frequency.

Additionally, since the Analog-to-Digital converter 209 is constructed to simultaneously perform the QPSK demodulation and Analog-to-Digital conversion, the number of circuit devices can be reduced and the circuit design can be simplified, resulting in a reduction of the power consumption, manufacturing costs, as well as overall size.

Moreover, since the digital FIR low-pass filter is used, phase linearity of the signal and noise reduction characteristics can be obtained.

Also, by using a Field Programmable Gate Array (FPGA), the alteration of the clock that is being used and the specific coefficients of the FIR low-pass filter can easily be reorganized, thereby the embodiment of the present invention can be applied to the various communication systems that use QPSK.

The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.